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Inventor: Matsuo Ichikawa

Applicant: Kabushikikaisha Suwa Seikosha

Specification

Title of the Invention: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

What is claimed is:

1. A semiconductor integrated circuit device, in which an MOS field effect transistor is formed taking a polycrystalline silicone formed on an insulating film as a substrate, characterized in that an insulating film of a gate part has a two-layer structure of a silicon oxide film and a silicon nitride film.

2. The semiconductor integrated circuit device according to claim 1, wherein the film thickness of said silicon oxide film ranges from 30Å to 1000Å.

3. The semiconductor integrated circuit device according to claims 1 and 2, wherein the film thickness of said silicon nitride film ranges from 30Å to 1000Å.

Detailed Description of the Invention:

This invention relates to an MOS field effect transistor using a polycrystalline silicon formed on an insulating film as a substrate and particularly to the gate insulating film thereof.

The semiconductor integrated circuit device has been developed into micro-structure with the years, and especially the development of the semiconductor integrated circuit device taking an MOS field effect transistor as a constituent is remarkable.

Aligner technique, etching technique and device technique are further being advanced, and the development of micro-structure reaches below 2μ rule to get nearer to its limit at the mass production level. A three-dimensional semiconductor integrated circuit device in which elements are stacked up has been conceived far in advance, and various studies have been made in the respective fields. Under these circumstances, suddenly the study is becoming active.

Devices which adopt an MOS field effect transistor as a constituent are now developed. At present, there are many problems in practical applications, and among them, especially the major problem is that the withstanding pressure of a gate part on polycrystalline silicon is low. This results from that when the surface of the polycrystalline silicon is oxidized, the polycrystalline silicon is further crystallized by heat, so that the surface is projected and recessed, and a sharp projection is generated through an oxide film. Consequently, partially the oxide film is extremely reduced in thickness so that the withstanding pressure between polycrystalline silicon which becomes a substrate and an upper electrode is deteriorated to cause leaking.

This projection of the polycrystalline silicon is hardly caused on the phosphorus highly doped polycrystalline silicon, but easily caused on the boron doped polycrystalline silicon and non-doped polycrystalline silicon.

Fig. 1 shows an example.

As shown in Fig. 1, the reference numeral 1 is a Si substrate, 2 is a SiO_2 film, 3 is an N-type polycrystalline Si, 4 is a P-type polycrystalline Si, 5 is a gate oxide film, 6 is a P^+ polycrystalline Si electrode, 7 is an N^+ polycrystalline Si electrode, 8 is a P^+ polycrystalline Si source, 9 is P^+ polycrystalline Si drain, 10 is an N^+ polycrystalline Si drain, 11 is an N^+ polycrystalline Si source, 12 is an interlayer insulation film, 13 is an Al electrode, and 14 is a projection of the polycrystalline Si.

As shown in Fig. 1, a sharp projection occurs on the surface outside the high density N^+ doped polycrystalline silicon to cause inferior withstanding pressure and leaking.

The invention has effected improvements to overcome the above disadvantages, and it is an object of the invention to improve withstanding pressure and leaking characteristic by forming a nitride film before forming an electrode, and adding a layer where a projection does not grow to a gate film.

Fig. 2 schematically shows a partial section of a three- dimensional semiconductor integrated circuit device formed according to a method of the invention.

The invention will now be described.

As shown in Fig. 2, the reference numeral 21 is a Si substrate, 22 is a SiO_2 film, 23 is an N-type polycrystalline Si, 24 is a P-type polycrystalline Si, 25 is a gate oxide film, 26 is a P^+ polycrystalline Si electrode, 27 is an N^+ polycrystalline Si electrode, 28 is a P^+ polycrystalline Si source, 29 is a P^+ polycrystalline Si drain, 30 is an N^+ polycrystalline Si drain, 31 is an N^+ polycrystalline Si source, 32 is an interlayer insulation film, 33 is an Al electrode, and 34 is a projection of the polycrystalline Si. Further, the reference numeral 35 is a nitride film.

According to the method of the invention described above, a projection of the polycrystalline Si grows only in the gate oxide film, and it does not grow when the nitride film is formed. Withstanding pressure is increased by the nitride film and leaking characteristic is improved.

The optimum thickness of the lower oxide film ranges from 400 to 600 Å, and the suitable thickness of the nitride film ranges from about 200 to 400 Å.

Though the description of the invention deals with the case where polycrystalline Si of the SiO_2 film provided on the Si substrate is taken as a substrate, the

same is true for the case of using the polycrystalline Si formed on the insulating substrate itself, and also the same is true for the case of using as the substrate the polycrystalline Si further formed through an insulating film on a film where an element is provided.

Brief Description of the Drawings:

Fig. 1 schematically shows a section of a semiconductor integrated circuit device comprising an MOS field effect transistor using polycrystalline Si as a substrate according to the conventional method; and

Fig. 2 schematically shows a section of a semiconductor integrated circuit device comprising an MOS field effect transistor using polycrystalline Si as a substrate according to the method of the present invention.